

NASA TECH BRIEF

Ames Research Center



NASA Tech Briefs announce new technology derived from the U.S. space program. They are issued to encourage commercial application. Tech Briefs are available on a subscription basis from the National Technical Information Service, Springfield, Virginia 22151. Requests for individual copies or questions relating to the Tech Brief program may be directed to the Technology Utilization Office, NASA, Code KT, Washington, D.C. 20546.

Differential Input Preamplifier

The problem:

To chop and amplify the very low level output of thermopile infrared detectors that will be used to measure the thermal energy flux of Jupiter and its departure from a blackbody spectrum. For subsequent synchronous demodulation, the output signal must have a negligible phase shift and very low input noise at the AC carrier frequency.

The solution:

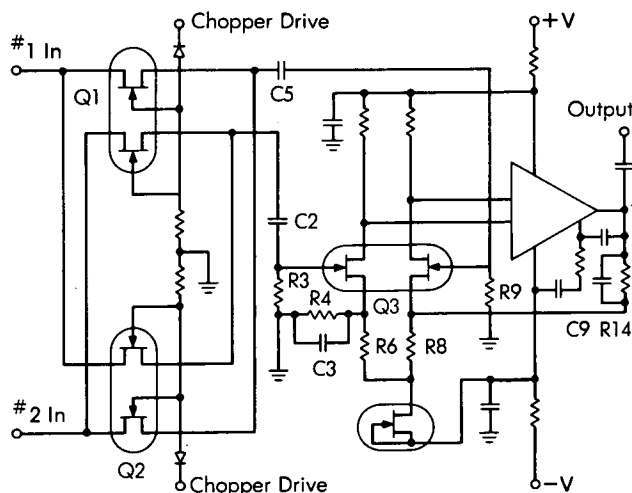
An amplifier which chops input signals (because the input signal levels are much lower than the input drift of available solid state devices); the resulting AC signal is RC-coupled to the input stage of other amplifiers.

How it's done:

The input DC signal is modulated full wave by two pairs of matched-junction field-effect transistors Q1, Q2. A two-phase chopper driver signal alternately turns off one pair of transistors with a reverse bias voltage and allows the other pair to conduct at zero bias. The signal input is reversed every half cycle, producing a full wave differential signal to the input RC coupling network (C2, R3, C5, R9).

The differential input signal is applied to the gates of a matched dual junction FET (Q3), which has excellent noise characteristics at low current. The amplified signal is applied to the input of a monolithic AC differential amplifier: closed-loop feedback is achieved by a feedback resistor between the output and the source connection of Q3. Closed loop gain is set by the ratio of the feedback resistor R14 to the Q3(2) source resistor R8. A matched network

(R4, R6) is used in the source connections to Q3 for maximum common mode rejection. It is possible to increase common mode rejection about 6 dB by trimming R4, but adequate rejection is achieved



without trimming and no adjustments are required. Closed-loop bandwidth is set by the R14, C9 time-constant to 40 kHz. Capacitor C3 is matched to C9 for increased high frequency rejection.

Notes:

1. Test results indicate that the amplifier has a 3-dB noise figure for source impedance of 15,000 ohms, improving with higher impedance. Common mode rejection is 94 to 100 dB without trimming. The power requirement is low, 0.6 mA from plus and minus 14-volt sources (17 mW).

(continued overleaf)

2. Requests for additional information may be directed to:

Technology Utilization Officer
Ames Research Center
Moffett Field, California 94035
Reference: TSP 72-10165

Patent status:

No patent action is contemplated by NASA.

Source: Paul W. Callaway of
Santa Barbara Research Center
under contract to
Ames Research Center
(ARC-10489)